

Notice of Allowability	Application No.	Applicant(s)	
	10/534,330	SCHEUCHER, HEIMO	
	Examiner	Art Unit	
	Tony Tran	2809	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 05/09/05.
2. ☒ The allowed claim(s) is/are 1-7.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. .
 3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
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| <ol style="list-style-type: none"> 1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date 20050509 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. 7. <input type="checkbox"/> Examiner's Amendment/Comment 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other _____. |
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Allowable Subject Matter

1. Claims 1-7 are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

For claim 1, the prior art of record Chittipeddi et al. (Patent Number 5751065) (hereinafter Chittipeddi), FIG. 2 teaches:

An integrated circuit (see the Abstract), having a substrate (substrate 201 – see e.g., [column 3, line 6]) and having a signal-processing circuit (a portion of the integrated circuit, including active devices such as field effect transistor 203 – see e.g., [column 3, lines 35-38]), which signal-processing circuit is produced in a region of the substrate adjoining a surface of the substrate and has a plurality of circuit elements (two field effect transistor 203s – see e.g., [column 3, lines 35-38]) and at least one first contact pad, wherein the first contact pad (metal layer 215 – see e.g., [column 3, lines 16-18]) has a first boundary face (see the shape of metal 215) accessible from outside the substrate (contact to metal 219 thru the two contact windows 255 – see e.g., [column 3, lines 13-15]) and a second boundary face (metal layer) opposite from the first boundary face, wherein the first contact pad (metal 215) is intended for the electroconductive connection of a component contact (window 255, metal 219 and wire 223) of a circuit component external to the integrated circuit to the signal-processing circuit, and having a protective layer

(dielectric layers 217 and 221) that is electrically insulating and provided on the surface of the substrate to protect the regions of the integrated circuit (a dielectric layer which is over the entire chip 1 – see FIG. 1, e.g., column 2, e.g., [lines 38-41]) covered by said protective layer, wherein for each first contact pad an aperture in the protective layer is provided, wherein for each first contact pad a second contact pad is provided that is of a height (?) of at least 15 um and is intended for direct connection to a component contact and extends through the relevant aperture (?) to the first contact pad and is electroconductively connected to the first contact pad and is seated on the protective layer by an overlap zone (?) that projects laterally beyond the aperture (?) and is closed on itself like a ring (note that patterned to cover the region 9 underneath the bond pads 3 is a ring like shape -- see FIG. 1, e.g., [column 2, lines 40-45]), wherein, along the whole of its ring-like extent, the overlap zone (?) projects beyond the aperture (?) laterally by substantially the same width of overlap (?), wherein the width of overlap (?) is in a range of between 2 um and 15 um (?), and wherein at least one element (?) of the signal-processing circuit is provided opposite the second boundary face of the first contact pad.

However, Chittipeddi fails to teach or render obvious of the relevant aperture, wherein for each first contact pad a second contact pad is provided that is of a specific height 15um, the overlap zone width in the range of between 2um and

15um and at least one element of the signal-processing circuit is provided opposite the second boundary face of the first contact pad.

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tony Tran whose telephone number is 571 270-1749. The examiner can normally be reached on Monday through Friday: 7:30AM-5:00PM (E.S.T.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Bruce can be reached on (571) 272-2487. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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DAVID BRUCE
SUPERVISORY PATENT EXAMINER